AMALITH: Advanced Mask Aligner Lithography

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As predicted by Moore's law, the number of components in integrated circuits is ever-growing. Since the mid-1970s the need of smaller and smaller feature sizes in semiconductor manufacturing has encouraged the development of new technologies as Lithography Projection Systems. Nevertheless, because of its comparatively low cost of ownership, versatility and easy handling, many companies, research centres and universities still employ Mask Aligners.

Advanced Mask Aligner Lithography (AMALITH) makes it possible to overcome some application limits for this technology, by introducing innovative concepts to shadow printing. This approach, in combination with lithography simulations, enables the use of Resolution Enhancement Technologies, already employed in front end processes.

We will show some application of complex mask layers based on Diffractive Optical Elements (DOE) as Fresnel Zone Plates or Diffractive Beam Splitters for process quality improvement and control. Optical Proximity Correction (OPC), Source Mask Optimization (SMO) and Phase-Shift Masks (PSM) have been used for increasing the process window, the resolution and the accuracy of the resulting photoresist profile.

1 Introduction

As already predicted by Moore's Law, the number of transistors that can be placed on an Integrated Circuit (IC) doubles approximately every two years. The shrinking of the components can lead to the employment of Next Generation Lithography (NGL) Tools and to the increase of the lithography steps per layer. In consequence the manufacturing costs for the new generation chips will dramatically increase. An advanced employment of mask aligners can prevent the switching to expensive higher-resolution projection lithography tools for some applications.

As shown in Fig. 1, the costs for mask aligner lithography for uncritical layers (> 5 µm resolution) are typically 3 times lower than in a low-cost stepper and about 5 times lower than in a wafer stepper from front-end. AMALITH® enlarges the application window in which mask aligners remain the most convenient fabrication approach.

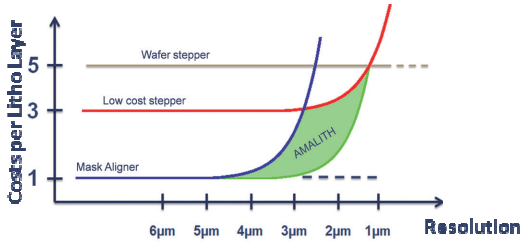

Fig. 1 *Scheme for the costs per lithography layer for Mask Aligners, low-cost Steppers and high-resolution wafer Steppers, related to the required resolution.*

The enabling technology for AMALITH® is a mask aligner equipped with MO Exposure Optics®. MOEO is an innovative illumination systems for mask aligners introduced by SUSS MicroOptics [1]. It allows to customize the angular spectrum of the light and provides a uniform and telecentric illumination on the mask plane. This is possible by including two microlens arrays as optical integrators and exchangeable Illumination Filter Plates (IFPs) in the light path.

In the following some results achieved by means of source mask optimization (SMO) technique will be shown.

2 Fresnel Zone Plate for TSV

A Fresnel-type OPC mask represents a lithography method that significantly improves the resulting contrast even for very large exposure gaps > 200 µm. Simulations and experiments have shown that customized illumination and Fresnel-type OPC structures allow to print vias for 3D IC and Through Silicon Via (TSV) at very large proximity gaps, e.g. a square shaped via of 11 x 11 µm at 800 µm gap [1], as the one shown in Fig. 2.

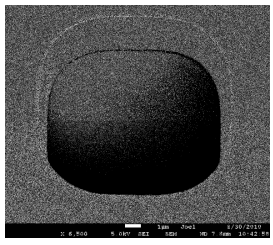

Fig. 2 *SEM picture of a via printed at 800 µm proximity gap in 5 µm thick AZ1518, using a square IFP. Feature size on the resist: 11 µm.*

3 *IFTA* for OPC Mask Design

In the previous example a simple analytic-type diffractive element was added to the mask layout. In the next example an iterative optimization algorithm was necessary in order to get the resulting OPC mask structure. The Iterative Fourier Transform Algorithm (IFTA) was run in order to optimize the final result on the resist, given by illuminating a cross shape mask (feature size: 10 µm) at 30 µm exposure gap (very common in production) with a wavelength of 365 nm. Before fabricating the optimized mask, simulation were done in order to assess the validity of this approach. Once this was demonstrated, test prints confirmed the expected improvement concerning the corner rounding and the sidewall shape, as shown in Fig. 3.

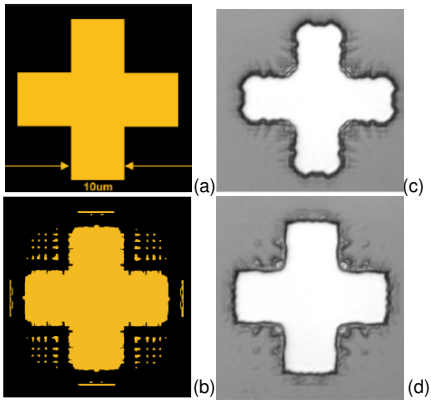

Fig. 3 *Original (a) and optimized (b) Mask Layout and resulting resist (0.98 µm, AZ1512) profile after development (c, d).*

4 *Phase-shift Mask*

One of the most important factors to determine the performance of the lithographic printing in a mask aligner is the resolution, which is limited by diffraction effects. Since in production a minimum gap is required in order to avoid damages and contacts between the mask and the wafer, it is very helpful to try to overcome the resolution limit for gaps > 30 µm. By adding phase information to a Lines and Spaces pattern, it was possible to get 2 µm wide lines at 30 µm exposure gap, where the typical resolution limit is about 5 µm. The operation principle and the printing results of this approach are shown in Fig 4, 5.

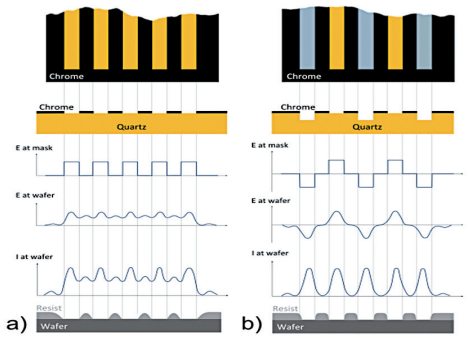

Fig. 4 *Resulting field and light propagation for Lines and Spaces binary (a) and phase shift (b) masks.*

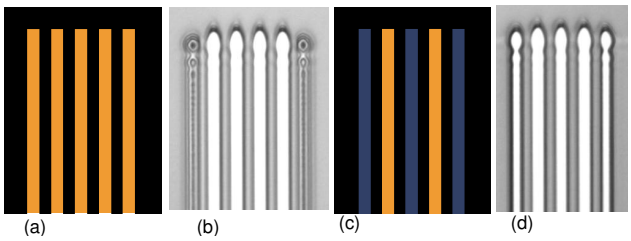

Fig. 5 *Resulting resist (0.98 µm, AZ1512) profile after development (b, d) for test prints done by using Lines and Spaces amplitude binary mask (a) and Phase-shift mask (c).*

At 30 µm gap, by using a simple amplitude mask, the resolution is too limited to reproduce the original structure on the resist layer. The added phase level (blue) made it possible to overcome the resolution limit and to get the wished five lines.

In order to evaluate the stability of this process, the Depth of Focus (DoF) was estimated. For this purpose, the same tests were repeated for exposure gaps changing between 25 µm and 50 µm. The DoF proved to be large enough to conclude that the process is stable and suitable for production environment, where gap variations are not always under control.

5 Passive Gap Sensor

A method for mapping the exposure gap uniformity in a certain process or machine consists in the integration on the mask layout of several diffractive beam splitters, which divide the incoming light in two tilted rays before reaching the coated wafer. The information concerning the gap is given by the measure of the distance between two developed points in the resist, provided by the incidence of the two rays themselves.

References

[1] R. Voelkel, U. Vogler, A. Bich, P. Pernet, K. J. Weible, M. Hornung, R. Zoberbier, E. Cullmann, L. Stuerzebecher, T. Harzendorf, and U. D. Zeitner, "Advanced mask aligner lithography: new illumination system", *Opt. Express 18, 20968-20978 (2010).*

[2] U. Vogler, F. Windrich, A. Schenke, R. Volkel, M. Bottcher, R. Zoberbier, "Cost-effective lithography for TSV-structures", *Electronic Components and Technology Conference (ECTC), IEEE 61st*, 1407-1411 (2011).

[3] R. Voelkel, U. Vogler, A. Bramati, T. Weichelt, L. Stuerzebecher, U. D. Zeitner, K. Motzek, A. Erdmann, M. Hornung and R. Zoberbier, "Advanced Mask Aligner Lithography (AMALITH)", SPIE 8326-69, Advance Lithography, San Jose, CA, USA, 13-16 February, 2012